CLAIMS

What is claimed is:

1. In a computer system having a processor executing at least one application program and a video decoder decoding a video data for display, an extraction circuit for extracting from the video data a plurality of header data each associated with one of a plurality of starting code types, the extraction circuit comprising:

a starting code detector receiving the video data, and operable to detect a starting code contained in the video data while the processor is executing the application program;

a branch circuit having an input connected to the starting code detector, and operable to branch the header data associated with the detected starting code type; and

a plurality of register units connected to the branch circuit for receiving the branched header data, each register unit being associated with one of the plurality of starting code types and each operable to store the header data associated with the register unit.

2. The extraction circuit according to claim 1, further comprising a calculator connected to the branch circuit and the plurality of register units, and operable to convert the header data into parameters usable by the video decoder and each register unit stores the parameters associated with the register unit.

3. The extraction circuit according to claim 1 wherein the starting code detector generates an interrupt for the processor when all header data are stored in the plurality of register units.

3.4. The extraction circuit according to claim 1 wherein the plurality of register units includes 3 register units respectively storing information related to a sequence header, group header and image header.

SUB B2

5. In a computer system having an application processor executing at least one application program and a video decoder decoding a video bitstream data for display, an extraction circuit for extracting from the video bitstream data a plurality of header data each associated with one of a plurality of header code types, the extraction circuit comprising:

a plurality of register units each associated with one of the plurality of header code types; and

a header processor having an input receiving the video bitstream data and an output connected to the plurality of register units, the header processor operable to detect a header code contained in the video bitstream data and upon detection route the associated header data to its output for storage by the register unit associated with the detected header code type, the header processor performing the detection and routing while the processor is executing the application program.

6. The extraction circuit according to claim 5 wherein the starting code detector generates an interrupt for the processor when all header data are stored in the plurality of register units.

SUB B3

7. In a computer system having a processor executing a plurality of programs and a video decoder decoding a video data for display, a method of extracting from the video data a plurality of header data each associated with a starting code, the method comprising the steps of:

receiving the video data containing the plurality of header data and the associated starting codes; and

repeating the following steps at least two times independent of the processor:

detecting a starting code in the received video data;

routing the associated header data to an associated one of the plurality of register units according to the detected starting code type; and

storing the associated header data in the associated register unit;

6 · 8. The method according to claim 5, prior to the step of storing, further comprising the step of converting the associated header data into parameters usable by the video decoder wherein each register unit stores the parameters of the associated header data.

9. The method according to claim 7, further comprising the step of interrupting the processor when all header data are stored in the plurality of register units.

10. A device for extracting parameters for decoding a video data flow, contained in headers coded according to an MPEG standard, said headers being preceded by a starting code, said device including means for organizing, independently and according to the starting code, a storage of the parameters in three register banks, and a starting code detector, implemented in wired logic and associated with a state machine for branching the contents of the headers to the register banks according to the starting code detected.

11. A device according to claim 10 wherein the state machine includes means for recognizing the occurrence of quantization tables in the data flow and for branching the data relative to these tables to a circuit for restoring quantization arrays.

12. A device according to claim 10 wherein the state machine is associated with a calculator for converting the data contained in the headers, prior to their storage in one of the three register banks, into instructions directly interpretable by a video decoder and accessible in any order by a microprocessor.

9 13. A device according to claim 10 wherein the detector is associated with a status register, accessible by a microprocessor and meant for containing the starting code detected.

9 14. A device according to claim 13 wherein the detector is associated with interrupt and stop registers for configuring its operating mode.

14

15. A device according to claim 14 wherein, in an automatic operating mode, the detector generates an interrupt for the microprocessor, only when all decoding parameters have been stored in the three register banks.

16. A device according to claim 14 wherein, in a manual operating mode, the detector generates an interrupt for the microprocessor, upon each occurrence of a starting code in the data flow.